Electronic Version
Stylesheet Version v1.1.1

[SPLIT-GATE NON-VOLATILE MEMORY]

Abstract

A split-gate non-volatile memory cell is described, including a substrate, a charge-trapping layer on the substrate, a split gate on the charge-trapping layer, and a source/drain in the substrate beside the split gate. The split gate includes at least one split region directly over the charge-trapping layer, and the charge-trapping layer around the split region serves as a coding region. A NAND non-volatile memory array is also described including the above-mentioned split-gate non-volatile memory cells that are arranged in a NAND-type configuration.